WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array in which a plurality of memory cells are arranged in a matrix, each storing n-valued data (n is a natural number equal to or larger than 2); and

a write circuit which writes data into each of the memory cells and which, before storing next at least one-valued data into a first memory cell in which j-valued data ($j < n$) has been stored in the memory cell array, writes j or less-valued data into at least one of the memory cells adjacent to the first memory cell.

2. The semiconductor memory device according to claim 1, wherein the write circuit, when writing j or less-valued data into at least one of the adjacent memory cells, writes the data at a first threshold voltage lower than that of the original data and, after having written the data into at least one of the adjacent memory cells, writes the data at a second threshold voltage higher than the first threshold voltage.

3. The semiconductor memory device according to claim 2, wherein the write circuit writes j-valued data in the first memory cell at a second threshold voltage higher than the first threshold voltage simultaneously with the operation of writing next at least one-valued data in the first memory cell.

4. The semiconductor memory device according to claim 1, wherein the memory cell array includes a second memory cell which acts as a flag and has at least a first and a second logic level.

5. The semiconductor memory device according to claim 4, wherein the memory cell array, when reading the first memory cell, carries out a read operation suitable for the first threshold voltage in a case where the second memory cell is at the first logic level and carries out a read operation suitable for the second threshold voltage in a case where the second memory cell is at the second logic level.

6. The semiconductor memory device according to claim 4, wherein the write operation, when writing j-valued data in the first memory cell at the second threshold voltage, writes data into the second memory cell and sets the second memory cell to one of the first and second logic levels.

7. The semiconductor memory device according to claim 4, wherein the write circuit, when writing (j + 1)-valued data into the first memory cell, writes data into the second memory cell and changes the logic level of the second memory cell from the first logic level to the second logic level.

8. The semiconductor memory device according to claim 5, wherein the write circuit, while writing j-valued data in the first memory cell at the second

threshold voltage and writing (j + 1)-valued data in the first memory cell, writes data into the second memory cell and changes the logic level from the first logic level to the second logic level.

9. The semiconductor memory device according to claim 5, wherein the memory cell array includes a plurality of second memory cells selected simultaneously with the first memory cell and, in a write operation, stores data of the same logic level into each of the second memory cells and, in a read operation, determines the first and second logic levels by a majority decision of the data read from said plurality of second memory cells.

10. The semiconductor memory device according to claim 1, wherein the adjacent memory cells are the memory cells adjacent to the first memory cell along a word line.

11. The semiconductor memory device according to claim 1, wherein the adjacent memory cells are the memory cells adjacent to the first memory cells along a bit line.

12. A semiconductor memory device comprising:

a memory cell array which has at least one first memory cell arranged in a matrix and at least one second memory cell selected simultaneously with the first memory cell, the first memory cell storing n-valued data (n is a natural number equal to or larger

than 2); and

a write circuit which, when writing next at least one-valued data into the first memory cell in which j-valued data ($j < n$) in the memory cell array has been stored, writes data to change the logic level of the second memory from a first logic level to a second logic level.

13. The semiconductor memory device according to claim 12, further comprising a read circuit which, when reading the data from the first memory cell, carries out a read operation suitable for j-valued data in the first memory cell in a case where the data in the second memory cell is at the first logic level and carries out a read operation suitable for data equal to or larger than $(j + 1)$ or more-valued data in the first memory cell in a case where the data in the second memory cell is at the second logic level.

14. The semiconductor memory device according to claim 12, wherein the write circuit has a data storage circuit and, when writing next at least one-valued data into the first memory cell in which the j-valued data ($j < n$) has been stored, stores data inputted from the outside world into the data storage circuit and causes the logic level of the data stored in the data storage circuit to be changed or remain unchanged on the basis of the data read from the first memory cell and further causes the data in the first memory cell to be changed

or remain unchanged on the basis of the data stored in the data storage circuit.

15. The semiconductor memory device according to claim 12, further comprising

a read circuit which, when reading (i + 1) or more-valued data in the first memory cell, makes the output data a specific value in a case where the second memory cell is at the first logic level.

16. A semiconductor memory device comprising:

a memory cell array which has at least one first memory cell arranged in a matrix and at least one second memory cell selected simultaneously with the first memory cell, the first memory cell storing k (k is a natural number equal to or larger than 2) bits of data; and

a write circuit which, when writing next at least one bit of data into the first memory cell in which i ($i < k$) bits of data has been stored in the memory cell array, writes data to change the logic level of the second memory cell from a first logic level to a second logic level.

17. The semiconductor memory device according to claim 16, further comprising

a read circuit which, when reading the data from the first memory cell, carries out a read operation suitable for i bits of data in the first memory cell in a case where the data in the second memory cell is at

the first logic level and carries out a read operation suitable for (i + 1) or more bits of data in the first memory cell in a case where the data in the second memory cell is at the second logic level.

18. The semiconductor memory device according to claim 16, wherein the write circuit has a data storage circuit and, when writing next at least one bit of data into the first memory cell in which the i (i < k) bits of data have been stored, stores an inputted data into the data storage circuit and causes the logic level of the data stored in the data storage circuit to be changed or remain unchanged on the basis of the data read from the first memory cell and further causes the data in the first memory cell to be changed or remain unchanged on the basis of the data stored in the data storage circuit.

19. The semiconductor memory device according to claim 16, further comprising

a read circuit which, when reading (i + 1) or more bits of data from the first memory cell, makes the output data a specific value in a case where the second memory cell is at the first logic level.

20. The semiconductor memory device according to claim 16, wherein

the memory cell array has a plurality of second memory cells selected simultaneously with the first memory cell and, in a write operation, stores data of

the same logic level into each of the second memory cells and, in a write operation, determines the first and second logic levels by a majority decision of the data read from said plurality of second memory cells.

21. The semiconductor memory device according to claim 16, wherein

the memory cell array has the second memory cell selected simultaneously with the first memory cell and a third memory cell, and

the write circuit, when writing next one bit of data into the first memory cell, writes data into the second memory cell and, when writing one bit of data following the next one bit of data into the first memory, writes data into the third memory cell.

22. The semiconductor memory device according to claim 16, further comprising

a read circuit which, when reading the data from the first memory cell, carries out a read operation suitable for i bits of data in the first memory cell in a case where the data in the second memory cell is at the first logic level, carries out a read operation suitable for (i + 1) bits of data in the first memory cell in a case where the data in the second memory cell is at the second logic level and the data in the third memory cell is at the first logic level, and carries out a read operation suitable for (i + 2) bits of data in the first memory cell in a case where the data in

the second memory cell is at the second logic level and the data in the third memory cell is at the second logic level.

23. The semiconductor memory device according to claim 21, wherein

the memory cell array has a plurality of second memory cells selected simultaneously with the first memory cell and a plurality of third memory cells,

the write circuit, when writing next one bit of data into the first memory cell, writes data of the same logic level into said plurality of second memory cells and, when writing one bit of data following the next one bit of data into the first memory, writes data of the same logic level into said plurality of third memory cells, and

the read circuit, when reading the data from the first memory cell, determines the first and second logic levels by a majority decision of the data read from said plurality of second memory cells and further determines the first and second logic levels by a majority decision of the data read from said plurality of third memory cells.

24. A semiconductor memory device comprising:

a memory cell which stores k bits (k is a natural number equal to or larger than 2);

a first storage circuit which stores an input data;

a second storage circuit which stores the data read from the memory cell or the input data; and

a control circuit which, in a write operation, holds or changes the data in the first storage circuit or the data in the second storage circuit on the basis of the data stored in the memory cell and which, in the middle of a write operation, inputs next write data to the first storage circuit, when the data stored in the first storage circuit becomes unnecessary to the write operation.

25. A semiconductor memory device comprising:

a memory cell array which has at least one first memory cell arranged in a matrix and at least one second memory cell selected simultaneously with the first memory cell, the first memory cell storing k (k is a natural number equal to or larger than 2) bits of data;

a write circuit which, before storing next at least one bit of data into the first memory cell in which i bits ($i < k$) of data has been stored in the memory cell array, writes i or less bits of data into at least one of the memory cells adjacent to the first memory cell and, when writing one bit of data into the first memory cell, writes data into the second memory cell; and

a read circuit which, when outputting the data read from the first memory cell, controls the logic

level of the data to be outputted on the basis of the data stored in the second memory cell.

26. The semiconductor memory device according to claim 25, further comprising at least one third memory cell selected simultaneously with the at least one first memory cell.

27. The semiconductor memory device according to claim 26, wherein

the write circuit writes data into the second memory cell at the same time that it writes (i + 1) bits of data into the first memory cell and writes data into the third memory cell at the same time that it writes (i + 2) bits of data into the memory cell, and

the read circuit controls the output of the data read from the first memory cell on the basis of the data in the second and third memory cells.

28. A semiconductor memory device comprising:

a memory cell which stores a plurality of data items using a plurality of threshold voltages;

a first and a second data storage circuit which are connected to bit lines and which store data of a first or a second logic level on the basis of data supplied from the outside world and the data read from the memory cell;

a control circuit which carries out a first write operation to change the threshold voltage of the memory cell when the data in the first data storage circuit is

at the first logic level, carries out a second write operation when the data in the first data storage circuit is at the second logic level and the data in the second data storage circuit is at the first logic level, and does not change the threshold voltage when the data in the first data storage circuit is at the second logic level and the data in the second data storage circuit is at the second logic level,

which, in a first verify operation, changes the logic level of the data in the first data storage circuit to the second logic level when the data in the first data storage circuit is at the first logic level, the data in the second data storage circuit is at the first logic level, and the threshold voltage of the memory cell has reached a first verify potential, does not change the data in the first data storage circuit when the threshold voltage of the memory cell has not reached the first verify potential, does not change the data in the first data storage circuit when the data in the first data storage circuit is at the first logic level and the data in the second data storage circuit is at the second logic level, and does not change the data in the first data storage circuit and holds its logic level at the second logic level when the data in the first data storage circuit is at the second logic level, and

which, in a second verify operation, changes the

logic level of the data in the second data storage circuit to the second logic level when the data in the second data storage circuit is at the first logic level and the threshold voltage of the memory cell has reached a second verify potential, causes the data in the second data storage circuit to remain at the first logic level when the threshold voltage of the memory cell has not reached the second verify potential, and carries out a write operation until the data in the first data storage circuit has reached the second logic level and the data in the second data storage circuit has reached the second logic level.

29. The semiconductor memory device according to claim 28, wherein a change in the threshold voltage in the second write operation is smaller than a change in the threshold voltage in the first write operation.

30. The semiconductor memory device according to claim 28, wherein the second verify potential is higher than the first verify potential.